

Features

- 2CH: Dual Buck
- CH1 Buck: V_{IN} 4.5V-17V, 2A, 1.2MHz, ECOT Mode Control with Fast Transient Response, Continuous Conduction Mode (CCM)
- CH2 Buck: V_{IN} 4.5V-17V, 2A, 1.2MHz, ECOT Mode Control with Fast Transient Response, Continuous Conduction Mode (CCM)

Applications

- Digital Set-top Box (STB)
- Tablet Personal Computer (Pad)
- Flat-Panel Television and Monitor
- Wi-Fi Router / AP

General Description

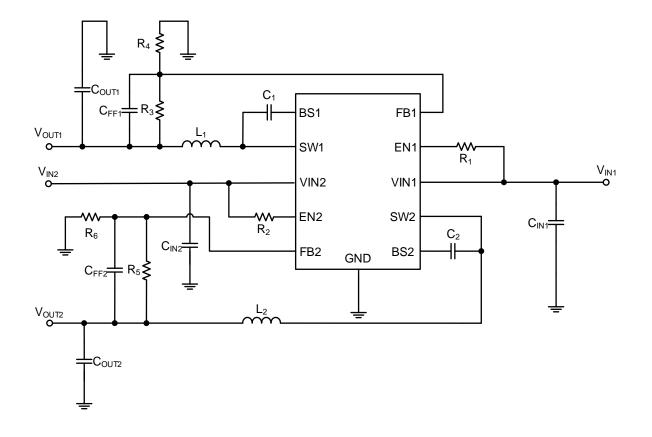
- Over Current Protection
- Over Voltage Protection
- Short Protection with Hiccup-Mode
- Thermal Shutdown
- Available in DFN10-3×3 Package
- -40°C to +85°C Temperature Range
- Digital Video Recorder (DVR)
- Portable Media Player (PMP)
- Cable Modem / XDSL
- General Purposes

The RY1228AD10 is a 2-channel PMU that includes dual high frequency, synchronous, rectified, step-down, switch-mode converters with internal power MOSFETs. Two inputs voltage range from 4.5V to 17V and two outputs with up to 2A current. ECOT control operation provides very fast transient response and easy loop design as well as very tight output regulation.

The RY1228AD10 requires a minimal number of readily available, external components and is available in an DFN10-3×3 package.



Typical Application Circuit

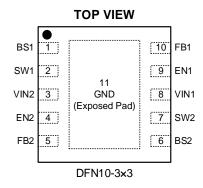


Basic Application Circuit



Pin Description

Pin Configuration



Top Marking: RY1228AD10YYLL (device code: RY1228AD10, YY=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	BS1	Bootstrap Pin for BUCK1. A capacitor connected between SW1 and BS1 pins is required to form a floating supply across the high-side switch driver.
2	SW1	Switching Pin for BUCK1.
3	VIN2	Power Supply Pin for BUCK2.
4	EN2	Enable Pin for BUCK2.
5	FB2	Feedback Pin for BUCK2. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
6	BS2	Bootstrap Pin for BUCK2. A capacitor connected between SW2 and BS2 pins is required to form a floating supply across the high-side switch driver.
7	SW2	Switching Pin for BUCK2.
8	VIN1	Power Supply Pin for BUCK1.
9	EN1	Enable Pin for BUCK1.
10	FB1	Feedback Pin for BUCK1. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
11	EPAD	Exposed Pad, ground pin.

Order Information

Marking	Part No.	Model	Description	Package	T/R Qty
RY1228AD10 <u>YYLL</u>	70303028	RY1228 AD10	RY1228AD10 2CH PMU, Dual Buck ECOT Force-CCM Buck, 4.5-17V, 2A, 1.2MHz, DFN10-3×3	DFN10- 3×3	3000PCS



Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V _{IN} , EN1, EN2 voltage	-0.3	18	V
SW1, SW2 voltage	-0.3	19	V
SW1, SW2 voltage (10 ns transient)	-5	20	V
BS1, BS2 voltage	-0.3	24	V
FB1, FB2 voltage	-0.3	6	V
Power dissipation ⁽³⁾	Internally Lim	ited	
Operating junction temperature, T _J	-40	150	°C
Storage temperature, T _{stg}	-55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J=160^{\circ}C$ (typical) and disengages at $T_J=130^{\circ}C$ (typical).

ESD Ratings

Item	Description	Value	Unit
	Human Body Model (HBM)		
V _(ESD-HBM)	ANSI/ESDA/JEDEC JS-001-2014	± 2000	V
	Classification, Class: 2		
	Charged Device Mode (CDM)		
V _(ESD-CDM)	ANSI/ESDA/JEDEC JS-002-2014	±200	V
	Classification, Class: C0b		
	JEDEC STANDARD NO.78E APRIL 2016		
ILATCH-UP	Temperature Classification,	±150	mA
	Class: I		

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature ⁽¹⁾	-40	125	°C
Operating temperature range	-40	85	°C
SYSTEM Input voltage V _{IN}	4.5	17	V
BUCK1 Output current	0	2	А
BUCK1 Output current	0	2	А

Note (1): All limits specified at room temperature ($T_A = 25^{\circ}C$) unless otherwise specified. All room temperature



limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information (1)(2)

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	45.5	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	15.9	°C/W
R _{0JB}	Junction-to-board thermal resistance	0.4	°C/W
ΨJT	Junction-to-top characterization parameter	15.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	2.8	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics (1) (2)

V_{IN} =12V, T_A =25°C, unless otherw	vise specified.

Parameter	Test Conditions	Min	Тур.	Max	Unit	
BUCK1						
Input Voltage Range		4.5		17	V	
Supply Current (Quiescent)	$V_{EN} = 3.0 V$		0.6	0.8	mA	
Supply Current (Shutdown)	$V_{EN} = 0$ or $EN = GND$			4	uA	
Feedback Voltage		0.588	0.600	0.612	V	
High-Side Switch On-Resistance	I _{SW} =100mA		110		mΩ	
Low-Side Switch On-Resistance	I _{SW} =-100mA		70		mΩ	
Valley Switch Current Limit		3			А	
Over Voltage Protection Threshold			18		V	
Switching Frequency		1.0	1.2	1.4	MHz	
Maximum Duty Cycle	V _{FB} =90%		94		%	
Minimum Off-Time			89		nS	
EN1 Rising Threshold				1.26	V	
EN1 Falling Threshold				0.8	V	
	Wake up V _{IN} Voltage		7.5		V	
Under-Voltage Lockout Threshold	Shutdown V _{IN} Voltage		4.5		V	
	Hysteresis V _{IN} voltage		3		V	
Soft Start			1.5		mS	
Thermal Shutdown			160		°C	
Thermal Hysteresis			30		°C	
BUCK2						
Input Voltage Range		4.5		17	V	
Supply Current (Quiescent)	V _{EN} =3.0V		0.6	0.8	mA	
Supply Current (Shutdown)	$V_{EN} = 0$ or $EN = GND$			4	uA	
Feedback Voltage		0.588	0.600	0.612	V	



High-Side Switch On-Resistance	I _{SW} =100mA		110		mΩ
Low-Side Switch On-Resistance	I _{SW} =-100mA		70		mΩ
Valley Switch Current Limit		3			А
Over Voltage Protection Threshold			18		V
Switching Frequency		1.0	1.2	1.4	MHz
Maximum Duty Cycle	V _{FB} =90%		94		%
Minimum Off-Time			89		nS
EN2 Rising Threshold				1.26	V
EN2 Falling Threshold				0.8	V
Under-Voltage Lockout Threshold	Wake up V _{IN} Voltage		7.5		V
	Shutdown V _{IN} Voltage		4.5		V
	Hysteresis V _{IN} voltage		3		V
Soft Start			1.5		mS
Thermal Shutdown			160		°C
Thermal Hysteresis			30		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.



Functions Description

The RY1228AD10 is a 2-channel PMU that includes dual high frequency, synchronous, rectified, step-down, switch-mode converters with internal power MOSFETs. The dual buck converters input voltage ranges from 4.5V to 17V and provide 2A continuous current. The output voltages can be adjusted by external resistor divider.

Buck1/Buck2 converter

The BUCK1/BUCK2 is an ECOT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.2MHz operating frequency to ensure a compact, high efficiency design with excellent performance.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to V_{FB} . When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 1.5ms.

Over Current Protection and Hiccup

The RY1228AD10 has cycle-by-cycle over current limit when the inductor current valley value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold. Once a UV is triggered, the RY9128D enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The RY1228AD10 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, V_{IN} low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.



Applications Information

Setting the Output Voltage

Each buck requires an input capacitor, an output capacitor, and an inductor. These components are critical to the performance of the device. It is internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

Take Buck1 as an example

$$V_{OUT} = V_{FB} \times \frac{R3 + R4}{R4}$$

V _{OUT} (V)	R1(KΩ)	R2(KΩ)	L1(µH)	C1(nF)	C _{IN} (µF)	C _{OUT} (µF)	C _{FF} (pF) Opt.
1.0	6.67	10	1.5	100	22	22×2	CFF Chapter
1.05	7.5	10	1.5	100	22	22×2	CFF Chapter
1.2	10	10	2.2	100	22	22×2	CFF Chapter
1.5	15	10	2.2	100	22	22×2	CFF Chapter
1.8	20	10	2.2	100	22	22×2	CFF Chapter
2.5	31.67	10	3.3	100	22	22×2	CFF Chapter
3.3	45	10	4.7	100	22	22×2	C _{FF} Chapter
5.0	73.33	10	4.7	100	22	22×2	C _{FF} Chapter

All the external components are the suggested values, the final values are based on the application testing results.

Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.





Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For a better performance, use ceramic capacitors placed as close to SYSIN as possible and a 0.1μ F input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum at $V_{IN}=2V_{OUT}$ where $I_{CIN} = \frac{I_{OUT}}{2}$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when $V_{IN}=2V_{OUT}$, input voltage ripple reaches its maximum of $\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

There are some differences between different types of capacitors. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{OSC}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{OUT_MAX}) can be limited approximately with Equation:

$$C_{OUT_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{SS} / V_{OUT}$$



Where $L_{\text{LIM}_{AVG}}$ is the average start-up current during the soft-start period, and T_{SS} is the soft- start time. On the other hand, special attention should be paid when selecting these components. The DC bias of these

capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55° C to $+125^{\circ}$ C, will only vary the capacitance to within $\pm 15^{\circ}$. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55° C to $+85^{\circ}$ C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Feed-Forward Capacitor (CFF)

RY1228AD10 has internal loop compensation, so adding C_{FF} is optional. Specifically, for specific applications, if necessary, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (C_{FF}) in the feedback network is to improve the transient response or higher phase margin. For optimizing the feed-forward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feed-forward capacitor identified, the value of feed-forward capacitor (C_{FF}) can be calculated with the following equation:

$$C_{FF} = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

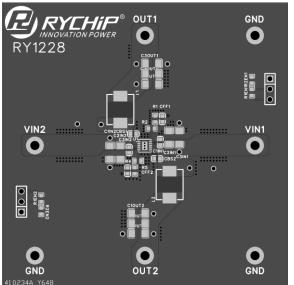
To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.



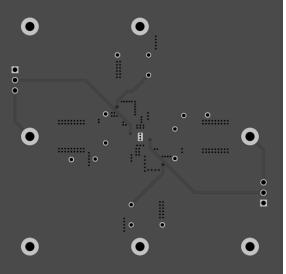
PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

- 1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
- 2. Bypass ceramic capacitors are suggested to be put close to the SYSIN Pin.
- 3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 4. VOUT, SW1/sw2 away from sensitive analog areas such as FB1/FB2.
- 5. Connect SYSIN, SW1/SW2, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer



Bottom Layer

ND

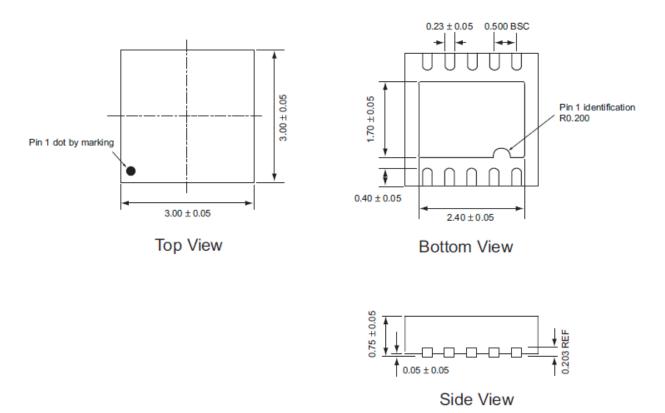
Sample Board Layout

Email: <u>support@rychip.com</u> ©RYCHIP Semiconductor Inc.



Package Description

DFN3*3-10



Note:

- 1. All dimensions are in millimeters.
- 2. Package length does not include mold flash, protrusion or gate burr.
- 3. Package width does not include flash or protrusion.
- 4. Lead coplanarity (bottom of leads after forming) shall be 0.10 millimeters max.
- 5. Pin 1 is lower left pin when reading top mark from left to right.